

Verilog Clock Task

I. Problem Statement

The assigned task was to design, implement, and test a clock module in Verilog.

II. Approach

The decision was made to generate a clock module which could be used in a variety of products by parameterizing the number of ticks which the clock will maintain its low and high values. In order to test this module, it was necessary to generate a testbench module which shows the operation of several clock. The test allows:

1. The clock to use its default values.
2. The clock have the number of ticks only when the signal is low changed.
3. The clock have the number of ticks only when the signal is high changed.
4. The clock have the number of ticks only when the signal is low or high both changed.

III. Solution

The assigned task was to design, implement, and test a clock module in Verilog. By using parameters for changes the number of ticks when the signal is low or high, it became easy to provide all of the variability that was desired.

Figure 1 demonstrates how the clock and testbench were synthesized and simulated. No special flags were used during synthesis or simulation. The output of the simulation shows that:

1. The clock (clock0) with default parameters has a period of 20 with the output being low for 10 ticks and high for 10 additional ticks.
2. The clock (clock1) have the number of ticks only when the signal is low changed has a period of 13 with the output being low for 3 ticks and high for 10 additional ticks.
3. The clock (clock2) have the number of ticks only when the signal is high changed has a period of 15 with the output being low for 10 ticks and high for 5 additional ticks.
4. The clock (clock3) have the number of ticks only when the signal is high changed has a period of 20 with the output being low for 11 ticks and high for 9 additional ticks.

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Command Prompt
Microsoft Windows [Version 6.1.7601]
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H:\>e:

E:\>cd UTD\201801\4341\Standards

E:\UTD\201801\4341\Standards>dir
Volume in drive E is TOSHIBA EXT
Volume Serial Number is 60EE-4CEF

Directory of E:\UTD\201801\4341\Standards

01/08/2018 12:09 PM <DIR> .
01/08/2018 12:09 PM <DIR> ..
01/08/2018 12:07 PM          3,642 a.out
01/08/2018 12:07 PM          2,796 ClockTest.v
09/07/2017 03:44 PM        14,575 Comment Standards.docx
01/08/2018 11:49 AM       186,084 Compile and Execute.jpg
01/08/2018 10:54 AM        13,437 Report Standards.docx
07/03/2016 12:27 PM         6,579 Report Standards.pdf
01/08/2018 11:47 AM       15,890 Verilog Comment Standards.docx
01/08/2018 11:47 AM       114,156 Verilog Comment Standards.pdf
01/08/2018 11:47 AM        13,438 Verilog Report Standards.docx
          9 File(s)        370,597 bytes
          2 Dir(s)    873,706,917,888 bytes free

E:\UTD\201801\4341\Standards>iverilog ClockTest.v

E:\UTD\201801\4341\Standards>vvp a.out
   0 clock0 = 0 clock1 = 0 clock2 = 0 clock3 = 0
   30 clock0 = 0 clock1 = 1 clock2 = 1 clock3 = 0
  100 clock0 = 1 clock1 = 1 clock2 = 1 clock3 = 0
  110 clock0 = 1 clock1 = 1 clock2 = 1 clock3 = 1
  130 clock0 = 1 clock1 = 0 clock2 = 1 clock3 = 0
  150 clock0 = 1 clock1 = 0 clock2 = 0 clock3 = 1
  160 clock0 = 1 clock1 = 1 clock2 = 1 clock3 = 1
  200 clock0 = 0 clock1 = 1 clock2 = 0 clock3 = 1
  250 clock0 = 0 clock1 = 1 clock2 = 1 clock3 = 0
  260 clock0 = 0 clock1 = 0 clock2 = 1 clock3 = 0
  290 clock0 = 0 clock1 = 1 clock2 = 1 clock3 = 0
  300 clock0 = 1 clock1 = 1 clock2 = 0 clock3 = 0
  310 clock0 = 1 clock1 = 1 clock2 = 0 clock3 = 0
  390 clock0 = 1 clock1 = 1 clock2 = 0 clock3 = 1
  400 clock0 = 0 clock1 = 0 clock2 = 1 clock3 = 0
  420 clock0 = 0 clock1 = 1 clock2 = 1 clock3 = 0
  450 clock0 = 0 clock1 = 1 clock2 = 0 clock3 = 0
  500 clock0 = 1 clock1 = 1 clock2 = 0 clock3 = 0
  510 clock0 = 1 clock1 = 1 clock2 = 1 clock3 = 1
  520 clock0 = 1 clock1 = 0 clock2 = 0 clock3 = 1
  550 clock0 = 1 clock1 = 1 clock2 = 1 clock3 = 1
  600 clock0 = 0 clock1 = 1 clock2 = 0 clock3 = 0
  650 clock0 = 0 clock1 = 0 clock2 = 0 clock3 = 0
  680 clock0 = 0 clock1 = 1 clock2 = 0 clock3 = 0
  700 clock0 = 1 clock1 = 1 clock2 = 1 clock3 = 0
  710 clock0 = 1 clock1 = 1 clock2 = 1 clock3 = 0
  750 clock0 = 1 clock1 = 1 clock2 = 0 clock3 = 1
  780 clock0 = 1 clock1 = 0 clock2 = 1 clock3 = 0
  800 clock0 = 0 clock1 = 0 clock2 = 0 clock3 = 0
  810 clock0 = 0 clock1 = 1 clock2 = 0 clock3 = 0
  850 clock0 = 0 clock1 = 1 clock2 = 1 clock3 = 0
  900 clock0 = 1 clock1 = 1 clock2 = 0 clock3 = 0
  910 clock0 = 1 clock1 = 0 clock2 = 0 clock3 = 1
  940 clock0 = 1 clock1 = 1 clock2 = 0 clock3 = 0
 1000 clock0 = 0 clock1 = 1 clock2 = 1 clock3 = 0

```

Figure 1 Synthesis and Simulation